WHAT IS CLAIMED IS:

1. Apparatus for providing well-matched source and sink currents, comprising:

a) a number of parallel current paths,

i) a first of which drives a first current mirror to mirror current to second and third of the parallel current paths;

ii) the second of which provides well-matched source and sink currents as outputs;

iii) the third of which is matched to the second;

iv) a fourth and fifth of which each comprise a transistor of a current steering mechanism and a bias transistor; wherein a first transistor of the current steering mechanism is coupled in the fourth current path and is driven by feedback from the third current path; wherein a second transistor of the current steering mechanism is coupled in the fifth current path and is driven by a reference voltage; wherein the bias transistor of the fourth current path mirrors current to the first current path under control of the current steering mechanism; and wherein the bias transistor of the fifth current path mirrors current to the second and third current paths under control of the current steering mechanism; and

b) a second current mirror, driven by a bias current, to mirror said bias current to each of the number of parallel current paths.

2. The apparatus of claim 1, wherein the first current mirror comprises an over-the-shoulder cascode current mirror.

3. The apparatus of claim 1, further comprising up/down current switches coupled to receive said source and sink output currents and pump up/down currents into a phase-locked loop in response to feedback received from the phase-locked loop.

4. The apparatus of claim 3, further comprising hardwired up/down current switches, coupled in the third current path and matched to the up/down current switches receiving said source and sink output currents.

5. The apparatus of claim 1, wherein the second current mirror comprises a transistor in each of the number of parallel current paths, each of which comprises a gate driven by the bias current, and each of which is coupled in one of the parallel current paths to sink current from the parallel current path.

6. The apparatus of claim 1, wherein the second and third parallel current paths comprise matched pairs of transistors, each matched pair being laid out using common centroid layout techniques.

7. The apparatus of claim 1, wherein the bias transistors of the fourth and fifth current paths mirror current to the first, second and third current paths by driving transistors in the first, second and third current paths;

and wherein the bias transistors are sized to about 25% of the driven transistors.

8. The apparatus of claim 1, wherein each of the second and third current paths comprises a pair of series transistors to source current to the current path; wherein first transistors of the series pairs form part of the first current mirror; and wherein second transistors of the series pairs are driven by the bias transistor of the fifth current path.

9. Apparatus for providing well-matched source and sink currents, comprising:

a) a first current path providing well-matched source and sink currents as outputs; the source current being provided through a first pair of series transistors;

b) a second current path, coupled in parallel with the first current path; the second current path comprising a second pair of series transistors, matched to the first pair of series transistors;

c) a first current mirror mirroring current to first corresponding transistors of the first and second pairs of series transistors;

d) a second current mirror mirroring current to second corresponding transistors of the first and second pairs of series transistors;

e) a current steering mechanism receiving a feedback signal from the second current path, as well as a reference signal, and steering current between the first and second current sources to match the feedback signal to the reference signal; and

f) a third current mirror mirroring a bias current to the first and second current paths, the first current mirror, and the current steering mechanism.

10. The apparatus of claim 9, wherein the first current mirror is an over-the-shoulder cascode current mirror.

11. The apparatus of claim 9, wherein corresponding transistors in the first and second current paths are laid out using common centroid layout techniques.

12. The apparatus of claim 9, further comprising up/down current switches coupled to receive said source and sink output currents and pump up/down currents into a phase-locked loop in response to feedback received from the phase-locked loop.

13. The apparatus of claim 12, further comprising hardwired up/down current switches, coupled in the second current path and matched to the up/down current switches receiving said source and sink output currents.

14. A method for providing well-matched source and sink currents, comprising:

a) mirroring a bias current to each of a number of parallel current paths of a circuit;

b) mirroring the bias current again, from a first of the parallel current paths to second and third of the parallel current paths; the second and third current paths being matched;

c) providing a reference voltage, and feedback from the circuit, to a current steering mechanism comprising fourth and fifth of the parallel current paths;

d) steering current between the first, second and third current paths by means of the current steering mechanism; and

e) outputting well-matched source and sink currents from the second current path.

15. The method of claim 14, further comprising, in response to feedback received from a phase-locked loop, outputting the source and sink currents to the phase-locked loop.

16. The method of claim 15, further comprising hardwiring up/down current switches in the third current path; the construction of the up/down current switches being similar to that used to implement switches that output the source and sink currents to the phase-locked loop.

17. The method of claim 14, further comprising, matching pairs of transistors in the second and third current paths, and laying out each matched pair of transistors using common centroid layout techniques.

18. The method of claim 14, wherein the provided feedback is derived from the third current path.